



# IEEE DASC 1076.1 Working Group

<http://www.eda.org/vhdl-ams/>

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# SAE Efforts Related to VHDL-AMS

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## ◆ SAE Statistical Modeling Working Group

- Participants from Ansoft, Fraunhofer Institute, Mentor Graphics, Synopsys
- Charter is to develop a generic approach for statistical modeling
  - Emphasis is on statistical modeling for Monte Carlo simulation
- Delivery consists of packages and documentation
- Status
  - Requirements collected and approved
  - General approach (package architecture) approved
  - Package content defined and mostly available in a draft implementation
  - Documentation outline being reviewed
- Contact David Smith, [dwsmith@synopsys.com](mailto:dwsmith@synopsys.com)

## ◆ SAE VHDL-AMS Modeling Working Group

- Charter is to develop control systems models for automotive industry, with emphasis on power train applications
- Contact Orest Storoshchuk, [orest.storoshchuk@gm.com](mailto:orest.storoshchuk@gm.com)



# Future Language Direction

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- ◆ **Known requirements**
- ◆ **Suggestions for future functionality**
- ◆ **Current activities**
- ◆ **Outline of future work**



# Requirements Known to WG

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## ◆ Unaddressed requirements from original language design

- DO21: Access to objects local to a design unit (circumventing ports)
  - Rejected as it violates VHDL philosophy
- DO23: Frequency-dependent models
  - Support for frequency-dependent independent sources provided
  - General support postponed since general frequency-dependent models have no closed form representation in time domain
- DO31: Dimensional analysis
  - Postponed as it requires changes to VHDL type system
- DO32: Default conversion between analog and digital ports
  - Postponed due to complexity



# Suggestions for Future Work (1)

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- ◆ **Language semantics to sweep parameters (Nokia)**
  - Seems to be related to corner modeling, needs further investigation
- ◆ **Table data types (Deepika Devarajan, Ansoft)**
- ◆ **Table lookup functions (IBIS)**
  - Need something similar to Verilog-AMS \$table\_model function
  - Multi dimensional (up to 4D)
  - Options for different interpolations (linear, spline, etc...)
- ◆ **Evaluation of strings passed as generics (IBIS)**
  - For example, pass a string generic (file name?) and evaluate it as part of a code expression later in the file
  - “Hard-coding” prevents re-use of code for multiple models
- ◆ **Model translation (IBIS)**
  - Verilog-AMS to VHDL-AMS and vice-versa



# Suggestions for Future Work (2)

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- ◆ **IP Protection (Deepika Devarajan, Ansoft)**
  - Need ability to deploy models in source form while keeping IP protected
  
- ◆ **Standard symbol format (Deepika Devarajan, Ansoft)**
  - This is an important issue for VDA and SAE
  
- ◆ **Vector/matrix arithmetic (Ernst Christen, Synopsys)**
  - Required for efficient and portable support of quantity and terminal arrays
  
- ◆ **Temperature relaxation models (Alex Zamfirescu, ASC)**
  - Needs further clarification



# Activities in Response to Requirements

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## ◆ Original Requirements

- DO21: VHDL 200X investigation to support XMR (cross model reference): FT7
  - Two approaches studied: alias based (any object declarable at DU level), package based (signals only)
  - Package based approach favored, but incomplete
  - Can be extended to quantities and terminals
- DO23: Uwe Feldmann (Infineon)
  - Upcoming white paper on RF modeling (nonlinear frequency domain)
- DO32: FDL'04 paper on Mixed Nets, Conversion Models and VHDL-AMS by John Shields, Ernst Christen. (Also in upcoming Kluwer book)
  - Introduces a new object: the structural wire
  - Wires have a shape
  - Wire views provide access to the wire as a signal, quantity, or terminal
  - Wire becomes signal, quantity, or terminal, depending on its views
  - Requires additional steps in elaboration



# Triage of Suggestions

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	<b>Assessment</b>	<b>Recommendation</b>
<b>Semantics for parameter sweep</b>	<b>Candidate for lang. extension</b>	<b>Need white paper defining requirements and scope</b>
<b>Table data types Table lookup functions</b>	<b>Candidate for package</b>	<b>Need white paper defining requirements and scope</b>
<b>Evaluation of strings</b>	<b>Candidate for lang. extension</b>	<b>Need white paper defining requirements and scope</b>
<b>Language translation</b>	<b>Vendor issue</b>	<b>Reject</b>
<b>IP protection</b>	<b>VHDL issue</b>	<b>Forward to Accellera</b>
<b>Standard symbol format</b>	<b>Outside WG scope</b>	<b>Reject</b>
<b>Vector/matrix arithmetic</b>	<b>Candidate for package</b>	<b>Need white paper defining requirements and scope</b>
<b>Temperature relaxation models</b>	<b>Candidate for package</b>	<b>Need white paper defining requirements and scope</b>



# Future Technical Activities

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- ◆ **Complete 1076.1 revision ballot**
  - Resolution of IRs, Errata
  - LRM updates
  - Ballot resolution
  
- ◆ **Convert suggestions to requirements**
  - White papers
  
- ◆ **Work with WG to set priorities**
  - Known and future requirements
  
- ◆ **Define new functionality according to priorities**
  - Language extensions
  - Packages



# Your Help Is Requested

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- ◆ **New requirements**
- ◆ **Early reviews of updated LRM for revision ballot**
- ◆ **IEEE revision ballot**
- ◆ **Future language definition work**
- ◆ **Development of standard packages**
- ◆ **Resolution of language issues**
- ◆ **Please contact WG Executive Committee**

