Workshop Title:
Beyond Syntax and Semantics: ***Industry Experiences with OVL/SVA/PSL***

Organizer: Harry Foster, Mentor Graphics Corporation; Accellera OVL committee Technical Advisor; IEEE P1850 WG Chair; Accellera UCIS member

Abstract:

With the emergence of assertion language and library standards—such as the IEEE SystemVerilog Assertions (SVA), the IEEE Property Specification Language (PSL), and the Accellera Open Verification Library (OVL)—many design teams are investigating the possibility of integrating both simulation and formal verification's assertion-based verification techniques into their flow. Yet successful application of these standards in an industrial setting requires additional project team member skills and verification process maturity beyond a simple understanding of assertion language syntax and semantics. Hence, this workshop shares multiple experiences of applying the assertion standards on various industry projects—with a focus on answering these questions:

- What is required to mature a project team's ABV skills for successful adoption?
- What needs to be considered in terms of a project's ABV infrastructure (beyond commercial tools)?
- What metrics need to be defined (and gathered) to measure progress?
- What benefits are real industry projects seeing using OVL/SVA/PSL?

While selecting a property and assertion language standard is an integral step for adopting assertion-based techniques, it is not the entire solution. Methodology is equally important to effectively applying ABV. In fact, without enforcing a consistent methodology across multiple design and verification engineers (for example, a consistent means of reporting errors, enabling or disabling assertions, and assigning actions performed upon error detection), the ad hoc use of assertions can end up being unmanageable and disruptive to the overall verification process. Hence, this highly interactive workshop is designed to address these methodology concerns through examples by experienced practitioners, allowing the attendee the opportunity to ask detailed methodological and process questions.

The workshop begins with a brief historical introduction to Accellera's assertion language and library standards. Next, we introduce assertion patterns and timing diagrams, which are a powerful project training tool for assertion specification. We then present details on the role that the OVL played as a key component of a formal property methodology for an ASIC project. We present statistics on the common patterns used on the project. Next, we share experiences of adopting a SystemVerilog assertion methodology within an existing mature ASIC/SoC ABV flow. We present best practices and methodological recommendations from this experience. Then, we present best practices and process improvement metrics from the use of PSL within an advanced ASIC/SoC flow. Finally, we discuss reuse strategies for creating assertion-based IP and conclude with a brief roadmap presentation on the assertion language and library standards.

Who Should Attend?

The workshop is intended to be highly interactive—allowing the attendee to ask detailed questions concerning developing a successful ABV methodology using OVL/SVA/PSL. We have created this workshop for many different audiences. For example:

- Novices in assertion-based techniques who might be an electronic engineering student learning about design and verification and interested in learning more about methodology from actual ABV experiences
- Academic instructors who are interested in integrating project methodology considerations into their discussions on assertion languages

- Experienced design or verification engineers who are considering adapting ABV on a future project and want to evaluate processes
- Design or verification managers whose goal is to improve the capability maturity of their organization through state-of-the-art industry best practices and processes

Speakers:

Harry Foster, Mentor Graphics Corporation, Addison, TX, USA
Mike Turpin, ARM Ltd., Cambridge, UK
Erik Seligman, Intel Corporation, Hillsboro, OR, USA
Mercedes Tan, Sun Microsystems, Santa Clara, CA, USA
Sivan Rabinovich, IBM, Haifa, Israel
Joe Richards, Broadcom Inc., Santa Clara, CA, USA

Outline: (Date: Monday June 9th, 2008, Time: 1pm-5pm, Meeting room: 207D)

Duration (minutes)	Session Title	Session Contents	Speaker
01:00-01:15	Welcome and Technical Overview	Workshop introduction, high-level overview of the Accellera's assertion standards, history	Harry Foster—Mentor Graphics, IEEE P1850 WG Chairman, Technical Advisor Accellera OVL committee
01:15-2:00	OVL Assertion Patterns and Timing Diagrams	Application of assertion patterns and timing diagrams: • Provides a useful visualization of common design behaviors and their appropriate assertion implementation • Provides a useful guide for selecting an appropriate OVL assertion checker	Mike Turpin – ARM, Accellera's OVL technical committee chair
2:00-2:45	Assertion Libraries and Methodology	The presenter shares his experience and recommendations adopting assertion libraries and assertion methodology to improve verification	Erik Seligman–Intel
2:45-3:00	Break		
3:00-3:45	Moving towards a SystemVerilog Assertions Methodology (SVA)	The presenter shares their previous and current ABV experiences, and then discusses strategies for adopting SVA within an organization	Mercedes Tan—Sun
3:45-4:30	Applied Property Specification Language (PSL)	The presenter shares his experience and recommendations for using Property Specification Language in an industrial setting	Sivan Rabinovich—IBM
4:30-5:00	Project Considerations	Project strategies and considerations for implementing an assertion-based verification methodology	Joe Richards--Broadcom
5:00-5:15	Summary and Future Direction for OVL/SVA/PSL	Concluding remarks and future directions	Harry Foster—Mentor Graphics, IEEE P1850 WG Chairman, Technical Advisor Accellera OVL committee